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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,342	10/07/2002	Jui-Lin Hung	9289-US-PA	2209

31561 7590 06/22/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
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EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,342	HUNG ET AL.	
	Examiner	Art Unit	
	John P. Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☒ Claim(s) *1,5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the applicant's amendment dated 5/5/2005.

The applicant amended claims 1-5 and 7.

Claims 1-9 are pending.

Response to Amendment

1. In view of the changes to the Specification and claims 3 and 7, the examiner withdraws the objections to the Drawings, and approves the changes. However, the examiner notes that there are additional objections to the claims (see below).

2. In view of the amendments to Claims 4 and 5, the examiner withdraws the rejections of said claims under 35 USC 112 second paragraph.

3. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new grounds of rejection (see below).

Claim Objections

4. Claims 1 and 5 are objected to because of the following informalities: Each claim should be corrected as follows: The phrase, "... replacing the faulty memory addresses by standby addresses ..." should instead recite, "... replacing the faulty memory addresses with standby addresses ...". Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. Claims 1, 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al., U.S. Patent No. 6240535.

As per Claim 1:

Farnworth et al. teaches a memory module testing/repairing method for testing and repairing a memory module (column 1 lines 20-24), comprising the steps of: testing the memory module (column 2 lines 48,49, column 3 line 12, FIG12A 164); registering faulty memory addresses in the memory module (column 3 lines 12-14, FIG.12A 166-168 and FIG.13A 180)); and "blocking" out address paths to the faulty memory addresses (FIG.13A 180, 182, 184) and replacing the faulty memory addresses by standby addresses (FIG.12B 170 and FIG.13A 186). The process of "blocking" faulty addresses is suggested where in steps 180, 182 and 184, where Farnworth et al. determines the failing address, latches the failing address, and blows the fuses for the failing address. In other words, the examiner recognizes this process as being a well known practice in the art of removing (blocking) addressing for the failing address by fuse blowing. And Farnworth et al., in column 1 lines 55-62, recites the advantage as a memory device and method for testing a chip after packaging. One with ordinary skill in the art at the time of the invention, would have found it obvious to adopt the circuit and method of Farnworth et al. in order to test chips after packaging, in order to provide a less expensive test-after-packaging solution.

As per Claim 2:

Farnworth et al. further teaches the memory module testing/repairing method of claim 1, wherein the step of blocking out fixed address paths to the faulty memory

addresses and replacing with specially selected standby addresses is carried out by blowing an electrical fuse (see Abstract and FIG.13A). And in view of the motivation previously stated, the claim is rejected.

As per Claim 4:

Farnworth et al. further teaches the memory module testing/repairing method of claim 1, wherein the method further includes setting the memory chip on the memory module into a testing mode (column 2 lines 48,49). And in view of the motivation previously stated, the claim is rejected.

2. Claims 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crump et al., U.S. Patent No. 5850562, in view of Farnworth et al., U.S. Patent No. 6240535.

As per Claim 5:

Crump et al. teaches a memory module testing/repairing device (FIG.2) for testing and repairing a memory module, comprising: a storage medium (FIG.3B, ROM 88) holding testing/repairing programs for testing and repairing the memory module (column 8 lines 6-13); and a main computer board having memory module slots therein (FIG.2 and FIG.3A 53) for accommodating memory modules (FIG.3A 54) and retrieving testing/repairing programs from the storage medium (column 15 lines 12-31) before carrying out a memory module testing/repairing procedure. Though Crump et al. teaches testing, it does not teach the actual repair, and the device as taught by Crump et al. has the capability to perform the repairs, as is taught by the analogous art of

Farnworth as follows: wherein the testing/repairing procedure further includes the following steps: testing the memory module (FIG.12A 164); registering faulty memory addresses in the memory module (FIG.12A 166, 168); setting a memory chip on the memory module to a testing mode (FIG.12A 160, 162); blocking out address paths to faulty memory addresses (FIG.13A 180, 182, 184) and replacing the faulty memory addresses by standby addresses (FIG.13A 186, 188, 190, 192); and setting the memory chip on the memory module back to a normal operation mode (column 4 lines 42-52). The process of "blocking" faulty addresses is suggested where in steps 180, 182 and 184, where Farnworth et al. determines the failing address, latches the failing address, and blows the fuses for the failing address. In other words, the examiner recognizes this process as being a well known practice in the art of removing (blocking) addressing for the failing address by fuse blowing. And, in view of the motivation for Farnworth et al. previously stated, the claim is rejected.

As per Claim 6:

Crump et al. further teaches the memory module testing/repairing device of claim 5, wherein the storage medium is a system having a floppy disk and a floppy disk reader (FIG.3B 84 Floppy). And, in view of the motivation previously stated, the claim is rejected.

As per Claim 7:

Crump et al. further teaches the memory module testing/repairing device of claim 5, wherein the storage medium is a hard drive system (column 1 lines 15-38). And, in view of the motivation previously stated, the claim is rejected.

As per Claim 8:

Crump et al: further teaches the memory module testing/repairing device of claim 5, wherein the storage medium is a system having an optical disk and an optical disk reader (column 4 lines 21-41). And, in view of the motivation previously stated, the claim is rejected.

As per Claim 9:

Crump et al. further teaches the memory module testing/repairing device of claim 5, wherein the device further includes a display monitor for displaying testing/repairing results (FIG.3B 106a). And, in view of the motivation previously stated, the claim is rejected.

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al., U.S. Patent No. 6240535, and further in view of Sher et al., U.S. Patent No. 6154851. Farnworth et al. fails to further teach the memory module testing/repairing method of claim 1, wherein the step of testing the memory module includes writing data into each memory address and reading data from the memory address and confirming the validity of the read-out data. But in an analogous art, Sher et al. does teach this feature in column 6 lines 44-55. And column 1 lines 65-68 and column 2 lines 1-2, the advantage of the invention is the capability to test and repair memory modules in a personal computer without removing the memory. One with ordinary skill in the art at the time of the invention, motivated as suggested, would combine the test method of Sher et al. with the test method of Farnworth in order to repair memory modules in a PC.

Conclusion

Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP§706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

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